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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/353,847	07/15/1999	HYUN CHANG LEE	8733/PD-6981	4171

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EXAMINER
ANYASO, UCHENDU O

ART UNIT	PAPER NUMBER
2675	14

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/353,847	LEE ET AL.	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. **Claims 1-26** are pending in this action.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. **Claims 1-26** are rejected under 35 U.S.C. 102(e) as being anticipated by Moon et al (US Patent 5,793,346).

Regarding **independent claims 1, 9, 11** and **19**, and for **claims 4-8** and **10**, Moon teaches a circuit and method of clearing a TFT LCD when the external power is removed from the liquid crystal display (column 1, lines 6-12).

Furthermore, Moon teaches a liquid crystal display device, comprising a plurality of data lines, a plurality of thin-film transistor (TFT) liquid crystal display cells electrically coupled to said plurality of data lines and arranged as a first string of TFT display cells electrically coupled

together by a first gate line and a second string of TFT display cells electrically coupled together by a second gate line, said second string of TFT display cells comprising respective support capacitors therein electrically coupled to said first gate line (column 4, lines 37-48).

Furthermore, Moon teaches a screen clearing circuit 40 connected at an input to the gate driving circuit 10 wherein the controller 30 controls gate driving circuit 10, which supplies gate on/off voltages sequentially through the gate lines to the thin film transistors 70 (column 4, lines 12-23, figure 6 at 10, 30).

Furthermore, the gate on/off generator 50 generates the Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50) wherein the screen clearing circuit 40 is connected to the Voff output of gate on/off generator 50 (column 4, lines 25-26). When the external power is disconnected, the screen clearing circuit 40 operates to discharge the storage capacitors 80 connected to the gate lines (column 4, lines 27-29). Elimination of the residual image improves the quality of TFT LCDs. This invention may be used in a wide variety of display devices such as notebook computers, handheld devices, and flat panel television screens (column 4, lines 33-36).

(column 4, lines 33-34)

Regarding **claims 2** and **3,** in further discussion of claim 1, Moon teaches how the first voltage level has a lower voltage level than a minimum value of the image signals (*see* figure 5; *see also* Abstract).

Regarding **claims 12-18, 20-26,** in further discussion of claims 11 and 19, Moon teaches an invention that comprises a capacitor of which one end is connected to the external power; a

diode of which the anode is connected to the other end of said capacitor, and the cathode is grounded; and a PMOS transistor of which the gate electrode is connected to the anode of said diode and the other end of said capacitor, the source electrode is grounded, and the drain electrode is connected to one end of a support capacitor of a TFT LCD (column 2, lines 10-27).

Furthermore, Moon teaches a means for detecting whether external power has been shut off; charging the support capacitor if the external power is not shut off, and then returning to the first detecting step; discharging the support capacitor if the external power is shut off, and then returning to the first detecting step (column 2, lines 28-35).

Response to Arguments

4. Applicant's arguments filed May 6, 2003 have been fully considered but they are not persuasive.

Regarding independent claims 1 and 9, Applicant argues that Moon does not teach a "level shifting means ... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off," and a "power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistor to the gate lines upon power." These assertions are not persuasive because Moon teaches gate on/off voltages within a liquid crystal display device, comprising a plurality of data lines, a plurality of thin-film transistor (TFT) liquid crystal display cells wherein a screen clearing circuit 40 is connected at an input to the gate driving circuit 10 such that the controller 30 controls gate driving circuit 10, which supplies gate on/off voltages sequentially through the gate lines to the thin film transistors 70

(column 4, lines 12-23, figure 6 at 10, 30). Furthermore, the gate on/off generator 50 generates the Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50). This facilitates the elimination of the residual image improves the quality of TFT LCDs.

Regarding independent claims 11 and 19, applicant argues that Moon does not teach "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output." This assertion is not persuasive because Moon teaches how a gate on/off generator 50 generates V_{off} and V_{on} voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50). This facilitates the elimination of the residual image improves the quality of TFT LCDs.

As such, Moon hones in on Applicant's invention by teaching each and every element of the claimed invention.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

07/07/2003

DENNIS-DOON CHOW
PRIMARY EXAMINER